

REMARKS/ARGUMENTS

Claims 1-20 were pending. In the present response, the Applicants have not amended or altered any claims, leaving claims 1-20 pending in the present application for the Examiner's consideration.

In summary of the Office Action of September 19, 2005, the Examiner has:

I. objected to claims 3, 10, and 12 under 35 USC 112(2);

II. rejected claims 1-3, 8-14, 16, and 20 under 35 USC 102(b);

III. rejected claims 4-7, 15, and 17-19 under 35 USC 103(a) over Wallace; and

IV. rejected claims 6 and 15 under 35 USC 103(a) over Wallace in view of Cong et al.

The Applicants respectfully traverse the Examiner's objections and rejections.

I. Objection to claims 3, 10, and 12 under 35 U.S.C. §112(2)

The Examiner has objected to claims 3, 10, and 12 under 35 USC 112, ¶ 2, because the word "*attempting*" is not definite claim language. The Applicants respectfully disagree.

Paragraphs 23-28 describe the decomposition of functions. One skilled in the art would understand sufficient steps needed to accomplish a decomposition. Given the context of the specification, if one skilled in the art understands the steps to decompose a user function into smaller functions, then the person knows the steps involved in an attempt to decompose a user function whether it is successful or not.

Paragraph 53 states that "an *attempt* is made to decompose user function $J(X)$ into function $r(s1, s2, x0, x1, x6, x10)$, where $s1$ and $s2$ are first stage decomposition functions that receive input variables $x4, x5, x2, x7, x8, x9, x3$, and $x11$. Function r is a second stage

decomposed function that receives the outputs of functions s1 and s2 and input variables x0, x1, x6, and x10." At steps 251, Figure 2C shows an "*attempt* to decompose user function into smaller functions" and, at 252, a check to see if the decomposition was successful.

The term "attempting" with respect to decomposing a function is definite because one skilled in the art would understand sufficient steps needed to accomplish a decomposition. Additionally, one skilled in the art would recognize that the same or similar steps are actually performed even if the attempt to decompose a user function is not successful. Accordingly, Applicants respectfully request the withdrawal of this objection.

II. Rejection of claims 1-3, 8-14, 16, and 20 under 35 U.S.C. 102(b)

The Examiner has rejected claims 1-3, 8-14, 16, and 20 under 35 USC 102(b) as being anticipated by U.S. Patent no. 6,360,352 to Wallace.

Claim 1 is allowable as Wallace does not disclose or suggest each and every element of claim 1. For example, claim 1 recites "*determining whether the first set of decomposed functions can be implemented by one of a set of lookup table configurations for the programmable integrated circuit.*"

Wallace is directed to a technique for finding symmetric and equivalent input pins of a circuit so that the equivalent input pins may be swapped. *See Wallace*, column 2 lines 1-6. The netlist representation of a fanout-free region of the circuit is converted into a quasi-canonical form (QCF). *Id.*, column 8, lines 19-24. Examples of a canonical form are a truth table, a binary decision diagram, or a Boolean logic formula. *Id.*, column 4 lines 18-19 and column 10 line 37. The QCFs are then used to create a swap structure, Table 4, to identify which pins may be swapped. *Id.*, column 5 lines 34-37 and column 9 lines 21-29.

The conversion of a netlist to a QCF to a swap structure is simply a change in how the circuit is represented. "For example, a 3-input NOR gate with inputs a, b, and c will generate a QCF of: (AND (NOT a) (NOT b) (NOT c))." *Id.*, column 9 lines 9-11. "[T]he positive QCF: (OR (NOT A) (NOT B) (NOT C)) is used to build the initial function of the swap structure ... [as] shown in the following Table [1]." *Id.*, column 10, lines 36-40. "[T]he pin

properties listed in Table 4 represents a swap structure or simplified circuit, such as swap structure or circuit 120." *Id.*, column 12, lines 26-27.

Accordingly, a netlist, a QCF, and a swap structure are all abstract representations or functions derived from the same circuit. Whereas, a "lookup table" is a separate physical device that may be programmed to implement or replace different circuits or functions. A netlist, a QCF, or a swap structure is not a separate physical device that can implement the circuit, but each is the circuit. A circuit in any representation does not implement itself. In contrast, claim 1 recites "determining whether decomposed functions can be implemented by one of a set of lookup table configurations."

Even if a circuit could implement itself, because a netlist, a QCF, and a swap structure are each the circuit, there is no need to determine whether one could implement the circuit.

Furthermore, Wallace's discussion of LUTs and FPGAs is limited to creating a netlist from a circuit, which may contain a LUT. *See Wallace*, column 8, lines 8-19 and column 14, lines 11-23. Wallace does not teach or suggest a LUT that is not already contained within the circuit. Thus, as a circuit does not implement itself, Wallace does not teach or suggest taking a function, whether it is from a netlist, QCF, swap structure, or circuit, and determining whether the function can be implemented by a lookup table.

For at least these reasons, claim 1 is patentable over Wallace. As claim 1 is patentable, dependent claims 2-10 are also patentable for at least the same rationale.

Applicants submit that claim 11 should be patentable for at least the same rationale as discussed with respect to claim 1. As claim 11 is patentable, dependent claims 12-20 are patentable for at least the same rationale.

III. Rejection of claims 4-7, 15, and 17-19 under 35 USC 103(a)

Claims 4-7 are patentable as they depend from patentable claim 1.

Claims 15 and 17-19 are patentable as they depend from patentable claim 11.

Appl. No. 10/694,919
Amdt. dated March 17, 2006
Reply to Office Action of September 19, 2005

PATENT

IV. Rejection of claims 6 and 15 under 35 USC 103(a)

Claim 6 is patentable as it depends from patentable claim 1.

Claim 15 is patentable as it depends from patentable claim 11.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



David B. Raczkowski
Reg. No. 52,145

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
DBR:dbr
60637058 v1